# CLASS E HIGH-EFFICIENCY POWER AMPLIFIERS, FROM HF TO MICROWAVE

**Nathan O. Sokal, Design Automation, Inc.**
**4 Tyler Road, Lexington, MA 02173-2404, U. S. A.**
**Tel. +1 (781) 862-8998 Fax +1 (781) 862-3769 73507.247@compuserve.com**

## ABSTRACT

Class E power amplifiers [1]-[3] achieve significantly higher efficiency than for conventional Class B or C. Class E operates the transistor as an on/off switch and *shapes the voltage and current waveforms* to prevent *simultaneous* high voltage and high current in the transistor; that minimizes the power dissipation, especially during the switching transitions. In the published low-order Class-E circuit, a transistor performs well at frequencies up to about 70% of its frequency of good Class-B operation. An unpublished higher-order Class E circuit operates well up to about double that frequency. The paper covers circuit operation, explicit design equations for the low-order Class E circuit, optimization principles, and experimental results.

## I. "WHAT CAN CLASS E DO FOR ME?"

Typically, Class E amplifiers [1]-[3] can operate with power losses smaller by a factor of about 2.3, as compared with conventional Class B or C amplifiers using the same transistor at the same frequency and output power. For example, a Class B or C power stage operating at 65% collector or drain efficiency (losses = 35% of input power) would have an efficiency of about 85% (losses = 15% of input power) if changed to Class E (35%/15% = 2.3). Class E amplifiers can be designed for narrow-band operation or for fixed-tuned operation over frequency bands as wide as 1.8:1, such as 225-400 MHz. (If harmonic outputs must be well below the carrier power, *any amplifier* other than Class A or push-pull Class AB cannot operate over a band wider than about 1.8:1 with only one fixed-tuned harmonic-suppression filter.) Harmonic output is similar to that of Class B amplifiers. Another benefit of using Class E is that the amplifier is *a priori* designable; explicit design equations are available. The effects of components and frequency variations are defined *a priori* [3, Figs. 5 and 6] and [4], and are small. When the amplifier is built as designed, it works as expected, without "tweaking" or "fiddling."

## II. PHYSICAL PRINCIPLES FOR ATTAINING HIGH EFFICIENCY

Efficiency is maximized by minimizing power dissipation, while providing a desired output power. The largest power dissipation is usually in the RF power transistor: the product of transistor voltage and transistor current *at each point in time* during the RF period, integrated and averaged over the RF period. Although the transistor must sustain high voltage during *part* of the RF period, and must also conduct high current during *part* of the RF period, the circuit can be arranged so that *high voltage and high current do not exist at the same time*. Then the product of transistor voltage and current will be low *at all times* during the RF period. Fig. 1 shows conceptual "target" waveforms of transistor voltage and current that meet the high-efficiency requirements. The voltage-current product is low throughout the RF period because:

1. *"On" state:* The voltage is nearly zero when high current is flowing, *i.e.*, the transistor acts as a low-resistance "on" switch during the "on" part of the RF period.
2. *"Off" state:* The current is zero when there is high voltage, *i.e.*, the transistor acts as an "off" switch during the "off" part of the RF period.

*Switching transitions:* Although the designer makes the on/off switching transitions as fast as feasible, a high-efficiency technique must accommodate the transistor's practical limitation for RF and microwave applications: the transistor switching times will, unavoidably, be appreciable fractions of the RF period. We avoid a high voltage-current product during the switching transitions, *even though the switching times can be appreciable fractions of the RF period*, by the following two strategies:

3. The rise of transistor voltage is *delayed until after the current has reduced to zero.*
4. The transistor voltage returns to zero *before the current begins to rise.*

The timing requirements of 3 and 4 are fulfilled by a

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

suitable load network (the network between the transistor and the load that receives the RF power), to be examined shortly. Two additional waveform features reduce power dissipation:

5. The transistor voltage at turn-on time is nominally zero (or the saturation offset voltage for a BJT). Then the turning-on transistor does not discharge a charged shunt capacitance, thus avoiding dissipating the capacitor's stored energy of $CV^2/2$, $f$ times per second, where $C$ is the capacitance value, $V$ is the capacitor's initial voltage at transistor turn-on, and $f$ is the operating frequency.

6. The slope of the transistor voltage waveform is nominally zero at turn-on time. Then the current injected into the turning-on transistor by the load network rises smoothly from zero at a controlled moderate rate, resulting in low $i^2R$ power dissipation while the transistor conductance is building-up from zero during the turn-on transition, even if the turn-on transition time is as long as 30% of the RF period.

*Result:* The waveforms *never* have high voltage and high current *simultaneously*. The voltage and current switching transitions are *time-displaced from each other*, to accommodate transistor switching transition times that can be *substantial fractions of the RF period*, *e.g.*, turn-on transition up to about 30% of the period and turn-off transition up to about 17% of the period.

A Class E amplifier generates waveforms that approximate the conceptual "target" waveforms in Fig. 1. Fig. 2 shows actual voltage and current waveforms in the low-order Class E circuit of Fig. 3. Note that those actual waveforms meet all six criteria listed above and illustrated in Fig. 1. Higher-order versions of the circuit approximate more closely the target waveforms of Fig. 1, making the circuit even more tolerant of component parasitic resistances and nonzero switching transition times.

## III. EXPLICIT DESIGN EQUATIONS

The explicit design equations given below yield the low-order lumped-element nominal-waveforms Class E circuit that operates with the waveforms of Fig. 3. (Distributed-element circuits are discussed briefly at the end of Section V.) For lack of space, the equation for *a priori* prediction of efficiency is omitted, and the design equations are given without the terms that accommodate the nonzero turn-off transition time and the components' parasitic resistances. The full equations are available from the author. In the equations below, $V_{CC}$ is the dc supply voltage, $P$ is the output power delivered to the load resistance $R$, $f$ is the operating frequency, $C1$, $C2$, $L1$ (dc-feed choke), and $L2$ are the load network shown in Fig. 3, and $Q_L$ is the network loaded $Q$, chosen by the designer as a trade-off: Lower $Q_L$ gives a wider operating bandwidth and lower power losses in the parasitic resistances of the inductors and capacitors, but higher harmonic content of the output. In a nominal-waveforms circuit, the minimum possible value of $Q_L$ is 1.7879; the maximum possible value is less than the network's unloaded $Q$.

$$V_{CC} = (BV_{CEV}/3.56) \text{ (safety factor} < 1 \text{ for off-nominal)}$$

$$R = 0.5768\,(V_{CC} - V_{CE(sat)})^2 / P$$

$$L1 = \text{RFC with } X \text{ usually} > 10\,X_{C1}$$

$$L2 = Q_L R/2\pi f$$

$$C1 = [1/2\pi f R\ 5.447]\,[1 + 0.81\,Q_L/(Q_L^2 + 4)] + 0.7/(2\pi f)^2\,L1 \qquad (\text{transistor } C_{out} \text{ is part of } C1)$$

$$C2 = [1/(2\pi f)^2\,L2]\,[1 + 1.110/(Q_L - 1.7879)]$$

*Differences from conventional Class B and C:* The load network is not intended to provide a conjugate match to the transistor output impedance. The network design equations come from the solution of a set of simultaneous equations for the steady-state periodic time-domain response, of a network containing non-ideal inductors and capacitors, to periodic operation of a non-ideal switch at the input port, at frequency $f$, to provide (a) an input-port voltage of zero value and zero slope at transistor turn-on time, (b) a first-order approximation to a time delay of the voltage rise at transistor turn-off, and (c) a nearly sinusoidal voltage across the load resistance $R$, delivering a specified RF power $P$ from a specified dc supply voltage $V_{CC}$.

The transistor's operating locus on the $I_d/V_{ds}$ plane is not a straight line (resistance) or a tilted ellipse (resistance + reactance). The operation during the "on" state of the switch is a nearly vertical line whose lower end is at the origin (0, 0); the "off" state of the switch is a horizontal line whose left end is at the origin. By design, the operating locus avoids the remainder of the plane, the region of *simultaneous* high voltage and high current (= high dissipation and reduced efficiency).

## IV. OPTIMIZING EFFICIENCY

*Principles:* The highest efficiency is obtained by minimizing the *total* power dissipated while the amplifier is delivering a desired output power. That can be done by modifying the waveforms slightly away from the nominal ones shown in Fig. 2, allowing *some* of the components of power dissipation to increase, while having *other* components of power dissipation *de-*

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

*crease by larger amounts*. For example, allowing the minimum of the voltage waveform to be at about 20% of the peak voltage, instead of at zero, increases the capacitance-discharge power loss, but it reduces the rms/average ratio of the current waveform and the peak/average ratio of the voltage waveform. Both of those effects can be exploited to obtain a specified output power with a specified (safe) peak transistor voltage, with lower rms currents in the transistor, L1, L2, C1, and C2. That reduces their $i^2R$ dissipations. If their series resistances are large enough, the decrease in their $i^2R$ power losses can outweigh the increase of capacitance-discharge power loss.

The power loss in the transistor $R_{on}$ and in discharging a partially charged *C1* are not functions of the design frequency. For given types of C or L components, capacitor losses (including in transistor $C_{out}$) increase with design frequency, inductor core losses increase, and inductor winding losses decrease.

The optimum trade-off depends on the specific combination of parameter values of the types of components being considered in a particular design. (It does not vary appreciably from one unit to another of a given design.) No *a priori* explicit analytical method yet exists for achieving the optimum trade-off among all of the components of power loss. Optimization is a numerically intensive task, too difficult to do by explicit analytical methods. But computerized optimization is practical. Running on a 586/100-MHz computer; a commercially available program [4], developed specifically for high-efficiency power amplifiers, designs a nominal-waveforms Class E amplifier in a time too short to observe, simulates the circuit in 43 ms, and optimizes the design automatically, according to user-specified criteria, in about 15 seconds.

## V. APPLICABLE FREQUENCY RANGE IS ABOUT 3 MHz TO 5 (maybe 11) GHz

The Class E amplifier can operate at arbitrarily low frequencies, but below about 3 MHz, one of the three types of Class D amplifier (also switching-mode types) might be preferred because they can provide as good efficiency as the Class E, with about 1.6 times as much output power per transistor, but with the possible disadvantage that transistors must be used in pairs, *vs.* the single Class E transistor. Class E is preferable to Class D at frequencies higher than about 3 MHz, for its higher efficiency, easier driving of the transistor input port, and less-detrimental effects from parasitic inductance in the output-port circuit. The upper end of the useful frequency range for the low-order Class E is the frequency at which the achievable turn-off switching time is of the order of 17% of the RF period. In a Class B amplifier, the turn-off transition time is 25% of the period. Therefore a low-order Class E circuit will work well with a particular transistor at frequencies up to about 17%/25% = 70% of the frequency at which that transistor works well in a Class B amplifier. (Unpublished higher-order Class E circuits can operate efficiently at frequencies up to about double that of the low-order version.) Class-E circuits have been made successfully at frequencies up to 5 GHz [5]. Several microwave designers have reported achieving remarkably high efficiency by driving the amplifier into saturation and using a favorable combination of series L to the load resistance [6] or fundamental and harmonic load impedances [7]-[13]. (The authors of [6]-[13] found the favorable tuning condition by using an automatic tuner and/or a circuit-simulation program to make an exhaustive search over the multi-dimensional impedance space, rather than by *a priori* explicit design equations.) Secchi [6] and Mallet *et al* [7] provided oscillograms of their drain-voltage and collector-voltage waveforms. Inspection of the $V_{ds}$ waveform in [6, Fig. 2] shows the circuit operating in nominal-waveform Class E with $R_{DS(on)}$ = 2.7 V/0.688 A = 3.9 ohms. The waveforms in Fig. 2(b) of [7] are Class E, but with an unusually small conduction angle. Probably higher output power could be obtained by increasing the conduction angle and modifying the load-network impedance accordingly. This author does not know the operating mode of [8]-[13]; very likely those amplifiers are distributed-components versions (see below) of Class E, achieved empirically.

*Distributed vs. lumped components:* High-efficiency waveforms similar to those in Figs. 1 or 2 can be generated with lumped and/or distributed components. At a given frequency, the choice depends on the available components and the trade-offs among their sizes, costs, quality factors, and parasitic effects. [5] and [17]-[19] were transmission-line versions of Class E, operating at 5, 2, 1, and 0.5 GHz. The 5, 2, and 1 GHz circuits were designed *a priori* by explicit design procedures, worked as expected, and were operated and measured without experimental adjustment.

## VI. EXPERIMENTAL RESULTS, REFERENCES

Table I summarizes Class E performance achieved, from 44 kW PEP at 0.52-1.7 MHz to 0.61 W at 5 GHz.

*References:* An annotated 32-items References list is available from the author on request; please enclose a self-addressed stamped #10 (24 x 10.5 cm) envelope.

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

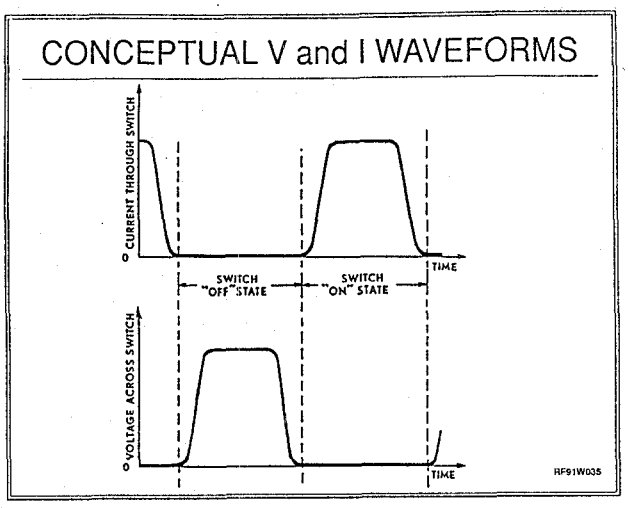


Fig. 1. Conceptual "target" waveforms.

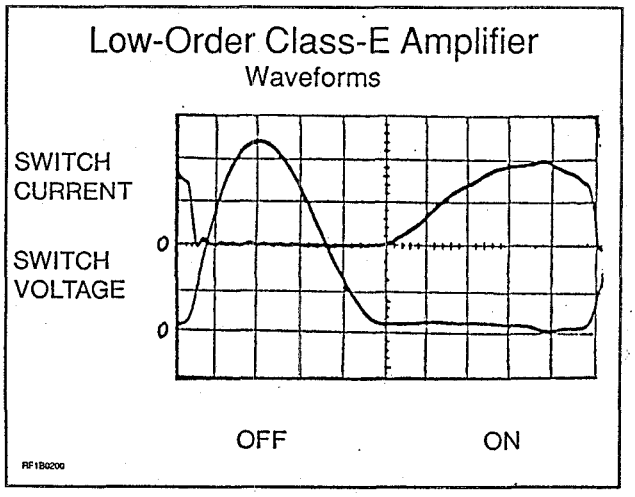


Fig. 2. Actual waveforms.

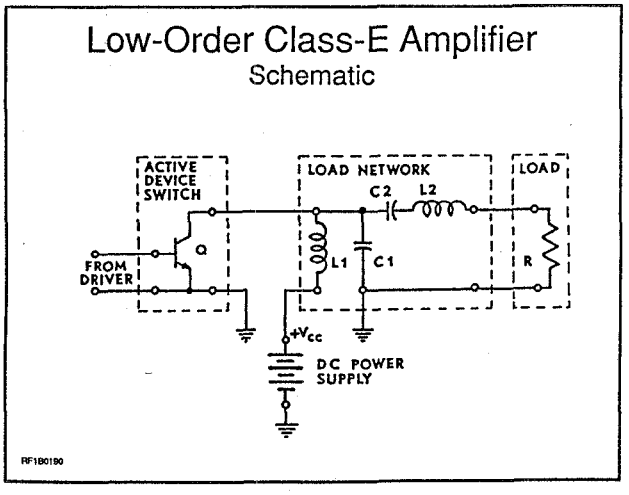


Fig. 3. Low-order Class E circuit.

**TABLE I. EXAMPLE CLASS E POWER AMPLIFIERS**

| Freq./Power | Transistor | Collector or Drain Eff'y/PAE | Organization | Approx. Year/ Reference No. |
|---|---|---|---|---|
| 0.52-1.7 MHz/44 kW PEP | push-pull MOSFETs | 95% | Broadcast Electronics, Inc. | 1992/[27] |
| 14 MHz/110 W | IRF540 | 92% | Design Automation, Inc. | 1986/[29] |
| 13.56 MHz, 27.12 MHz/2 kW | MOSFET | 90% | Dressler Hochfrequenztechnik | 1993 |
| 13.56 MHz/3 kW, 5.5 kW | MOSFET | ?% | Advanced Energy Industries, Inc. | 1992-97 |
| 27.12 MHz/22 W | IRF510 | 89-92% | Design Automation, Inc. | 1991/[30] |
| 145 MHz/2.58 W | Siliconix VMP4 VMOSFET | 96.5%/81.3%* | École Polytech. Féd. Lausanne | 1980/[25] |
| 300 MHz/30 W | push-pull BJTs | 89% | Harris RF Communications | 1992/[32] |
| 450 MHz/14.96 W | combine 4 modules MRF873 BJT | 89.5% | City Univ. of Hong Kong | 1997/[23] |
| 500 MHz/0.55 W | Siemens CLY5 GaAs MESFET | 83%/80% | Univ. of Colorado | 1995/[19] |
| 850 MHz/1.6 W | GaAs MMIC | 62.3% PAE | M/A-COM | 1994/[16] |
| 1 GHz/0.94 W | Siemens CLY5 GaAs MESFET | 75%/73% | Univ. of Colorado | 1995/[18], [17] |
| 2.45 GHz/1.27 W | Fujitsu FLC30 GaAs MESFET | 72% PAE | RCA David Sarnoff Res. Ctr. | 1981/ [6] |
| 2.45 GHz**/210 mW | Raytheon RPC3315 MESFET | 77%/68%/71%* | Design Automation, Inc. | 1979/[26] |
| 5 GHz/0.61 W | Fujitsu FLK052WG MESFET | 81%/72% | Univ. of Colorado | 1996/ [5], [19] |

**1/20 scaled-frequency model at 122.5 MHz; all L and C = 20X final values

*Overall eff'y = $P_{out}/(P_{dc} + P_{input\text{-}drive})$

0-7803-4471-5/98/$10.00 (c) 1998 IEEE